MATHEMATISCHES FORSCHUNGSINSTITUT OBERWOLFACH

T a g u n g s b e r i c h t 5o/1983

Mathematische Methoden zur VLSI

27.11 bis 3.12.1983

The first Oberwolfach Conference on 'Mathematische Methoden zur VLSI' was organized by M.J. Fischer (New Haven), M. Fontet (Paris) and G. Hotz (Saarbrücken).

The 29 participants came from 7 countries (FRG, USA, France, GDR, Israel, Netherlands and Switzerland).
The aim of this conference was to bring together people doing research in different areas being relevant for VLSI-design and VLSI-applications. The relatively small number of participants made it possible to spend a sufficient amount of time for each lecture including a very extensive discussion. This lead to a useful dialogue between people doing research in a more theoretical direction on the one side and in a more experimental direction on the other side.
It turned out, that a conference like this one should not be restricted to mathematical methods in VLSI, but it should consider methods and algorithms in the field of distributed computing too.
So all participants of the conference would greatly appreciate a next conference of this kind.
The 2o lectures given at the conference concerned the following fields:

- graph theoretical problems
- layout problems (geometry, topology)
- models, algorithms for parallel computation
- theoretical lower and upper bounds for VLSI algorithms
- methods for formal specification of VLSI algorithms
- data structures suitable for VLSI
- languages for network design and geometrical layout
- systems for chip layout
- simulation techniques
- testing problems

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Vortragsauszüge

K. MEHLHORN:

On Switchboxrouting

A switchbox routing problem is given as an n by m rectangular grid and a number of nets $N_1,\ldots,N_N$. A net is a pair of points on the boundary. A solution is a set $P_1,\ldots,P_N$ of pairwise edge-disjoint paths, one for each net. Path P_i connects the two terminals of net N_i. An algorithm is presented which finds a solution (if there is one) in time $O((n+m)\log(n+m))$. The algorithm finds a solution where each path P_i bends only $O(1)$ times on the average.

(joint work with F. Preparata)

A. ROSENBERG:

Embedding Graphs in Books

We consider the problem of embedding a graph in a book, with the vertices lying along the spine of the book and the edges on the pages: each edge lies on a single page, and edges on the same page don't cross. We seek embeddings that use few pages and that minimize the (cut)width of each page. Our main results:

(1) exhibit optimal embeddings of a variety of graph families;

(2) exhibit two cases of a "tight" pagewidth-pagenumber trade off;

(3) determine the effects of the structure of a graph on its pagenumber; e.g.: (1a) A graph with a size-B bifurcator can be embedded in $(2+\sqrt{2})B$ pages. (1b) There exist 3-page embeddable n-vertex graphs with size $\Omega(n/\log n)$ bifurca-

tors. (2a) Every valence-d n-vertex graph can be embedded in $\min(n/2, O(d\sqrt{n}))$ pages. (2b) There exist n-vertex valence-d graphs (for all large n and d>2) that require $\Omega(\frac{n^{1/2-1/d}}{(\log n)^{1+O(1)}})$ pages.

(joint work with F. Chung, T. Leighton)

B. BECKER:

On the Optimal Layout of Planar Graphs with Fixed Boundary

We consider the (optimal) layout of graphs with respect to very general cost functions including the p-th power of the usual Euclidian distance metric for p=2,3,.... For a large class of graphs, which occur f.e. in chip layout problems as the abstract structure of switching circuits, we show the existence and uniqueness of the optimal layout.
We get an interesting characterization of non planar layouts of planar graphs and show that the optimal layout of planar graphs is planar (or at least "nearly planar").
This property makes it possible to decompose the general layout problem into two independent problems: i) Find a layout of a circuit, which not necessarily is planar, but which has an "allowed crossing-behaviour"; ii) Take the crossing points as additional nodes of the graph and optimize. Our theorems show that thereby no new crossing points will be generated.

(joint work with G. Hotz)

A. CREMERS:

Algorithmic Notation for VLSI

A formal specification of a VLSI algorithm serves several important purposes. It provides a (executable) prototype, input to the implementation cycle, and a basis for the functional description of the device to the embedding environment. Based on the computational model of a data space

(transition system on a structured state space), an algorithmic notation is developed which combines the concept of state with techniques of functional programming. In this notation, state is defined in terms of an ensemble of data-defined functions of an associative store, and transitions are defined by means of expression-defined functions of a processor. The central notion of side-effect-free computation of transitions gives direct access to the application area of systolic algorithms. For locally synchronized algorithms the notation is extended by a simple data-flow scheme of communication (equivalencing of synchronized cells of the associative store). Examples are given from the areas of signal processing and sorting/searching.

(joint work with T.N. Hibbard)

A. BRYANT:

A Switch-level Model for MOS Digital Circuits

The switch-level model describes the logical behaviour of digital circuits implemented in Metal-Oxide Semiconductor (MOS) technology. A circuit is represented by a network of nodes connected by transistor switches. The model abstracts the actual electrical behaviour in 3 respects:

1. Nodes are assigned states form the set {0,1,X}, where X represents either an invalid or unknown voltage level.
2. The formation of logic states is described by a discretized model of transistor resistances and capacitances.
3. The sequential behaviour is represeneted by a sequence of states $\overline{y_0}, \overline{y_1}, \overline{y_2}, \ldots$ where $\overline{y_i}$ is computed from $\overline{y_{i-1}}$ by setting the transistors according to the states of their gate (control) nodes in $\overline{y_{i-1}}$, initializing the nodes to states in $\overline{y_{i-1}}$ and computing the "steady state response" function.

It is shown that the steady state response function can be computed in linear (in the number of transistors) time, and hence an efficient logic simulator can be implemented based on this model.

T. LENGAUER:

Delay-Independent Switch level Simulation of MOS Circuits

This work is based on the switch level model for MOS Circuits presented by R. Bryant at this meeting. This model does not contain any information about delays in the circuit and does not simulate circuit timing. In fact, in many applications, the delay information is not available to the designer at the time of simulation. However, if the circuit contains race conditions delays inside the circuit will not only affect circuit performance but also circuit functionality. We propose an extension of the model that quantifies over all possible assignments of delays to circuit components and returns a defined value on a wire only if this value is achieved independently from what the delays are in the circuit. We give an $O(n^2)$ (n= transistors) algorithm for computing the response of the circuit to a stimulus in this model. We increase the efficiency of the algorithm to $O(n\alpha(n))$ and $O(n)$ for special classes of networks.

(joint work with S. Näher)

F.P. PREPARATA:

Optimal Fastest Multiplier

According to VLSI theory, $[\log n, \sqrt{n}]$ is the range of computation times for which there may exist an AT^2-optimal multiplier of n-bit integers. Such networks were previously known for the time range $[\Omega(\log^2 n), O(\sqrt{n})]$. In this paper we settle this theoretical question, by exhibiting a class of AT^2-optimal multipliers with computation times $[\Omega(\log n), O(\sqrt{n})]$. These designs are based on the DFT on a Fermatring, whose elements are represented in a redundant radix-4 form to ensure $O(1)$ addition time.

(joint work with K. Mehlhorn)

J.E. SAVAGE:

SLAP - An Automatic System for VLSI Layout

SLAP is a fast method for translating Boolean equations into chip layouts. It parses Boolean equations and generates level graphs that are placed in the plane by collecting vertices at the same level into a single row and then routing between rows. A user may alter the layout without changing the initial functional specification by selecting from heuristics for changing the order of elements in rows, for giving a relative location to elements in adjacent rows and for changing the levels of elements.
We give a comparison of SLAP to Programmed Logic Arrays (PLA's) and Weinberger arrays and then analyse two problems arising in SLAP, the "row placement" and "row ordering" problem. Experiments with binary adders and multipliers, binary trees and meshes of trees, and analysis suggest that the methods described above have promise for silicon compilation.
(joint work with S.P. Reiss)

M. TCHUENTE:

On the Design of Efficient Systolic Algorithms

Most of systolic algorithms suffer from the drawback that the elementary cells are active only every k-th time step (where $k \geq 2$), which limits the degree of parallelism and increases the computation-time (such algorithms are said to be of efficiency 1/k). We propose an approach based on the classical divide-and-conquer technique, which, starting from an algorithm of efficiency 1/k, yields a new algorithm of efficiency one; this approach is illustrated on several examples. As a conclusion we suggest the following methodology for the design of efficient systolic algorithms:
1. First construct a simple (non systolic) solution
2. Use the technique introduced by C.E. Leisersen to derive

a k-slowed systolic algorithm

3. Construct a non-slowed systolic solution by applying the approach introduced here.

(joint work with Yves Robert)

J. van LEEUWEN:

Plane Realization of Three-Dimensional VLSI-Designs

We consider the problem of realizing a three-dimensional VLSI-design, consisting of v layers of area A each, in the plane. We use Thompson's grid-model for the surface of a (2-dim.) chip and, in three dimensions, its natural generalization with "cells" corresponding to unit size cubes. Thompson (1980) essentially observed that a three-dimensional VLSI-design of the given specification can be mapped to (i.e., laid out in) the two-dimensional plane in a rectangle of area $O(v^2A)$ but his argument is rather inaccurate. When done precisely, it shows a $9v^2A$ area bound. We show that (i) there is an embedding technique that (asymptotically) requires only $(1+\varepsilon)v^2A$ area for any $\varepsilon > 0$ and v large, and (ii) there are three-dimensional designs of v layers of area A each such that any realization in a two-dimensional plane requires $(1-\varepsilon)v^2A$ area for A sufficiently large. Thus the "v^2A" embedding method (constant of proportionality 1!) is worst case optimal, ignoring low order terms.

(joint work with H. Bodlaender et al.)

T. OTTMANN:

Skeleton Structures for Representing Sets of non Iso-oriented Objects

A number of techniques from Computational Geometry has been used in order to improve certain design tools for VLSI-circuits at least at the lowest design-level, the geometrical level. So far mainly problems involving sets of iso-oriented rectangles or x-y polygons have been studied. One reason for this fact is this: There are efficient data-structures and algorithms for the iso-oriented case, in particular wellknown skeletonstructures like the segment treee and interval (file-) tree. At first glance these structures do not have an analogue for sets of non iso-oriented objects. However, in this talk it is shown, that there is a uniform way of transferring line sweep algorithms and data-structures from the iso-oriented case to the non iso-oriented case. This is demonstrated by the "report intersecting pairs problem" which is the "report intersecting pairs of rectangles problem" in the iso-oriented case and the "report intersecting pairs of polygons problem" in the non iso-oriented case. The crucial notion in this context is the initial placement order for a given set of line segments in the plane which is suitable for a line sweep.

E.W. MAYR:

Techniques for Efficient Graph Algorithms in Parallel Environments

We present new paradigms for efficient parallel graph algorithms. These techniques are called "aliasing", "filtering" and "funnelled pipelining". They are used to derive efficient algorithms for several graph problems, like connected components, minimum spanning forests, and biconnected components.

The algorithms assume that the input is given in form of adjacency (weight) matrices, and they work in a when- and where-determinate fashion. The algorithms can be implemented in VLSI (using tree architectures), but also in architectures based on a bus- or Ethernet-like structure. Filtering is a process that transforms the input instances into smaller or simpler problems which still faithfully represent the original instance. For the minimum spanning forest and biconnected component problem the filtering is done in consecutive, more and more stages. Every subsequent stage requires double the effect of the previous, but it is also called upon only half as often. Thus, the stages can be combined into a "funnelled" pipeline whose overall period is still short. Filtering and funnelled pipelining are examples for techniques to spread the computational effort in parallel environments evenly, and to balance the costs for interprocessor communication and local memory size.

M.J. FISCHER:

On Distributed Consensus and its Implications for VLSI

We consider a system S of deterministic asynchronous processes $p_1,\ldots,p_n$ with corresponding input registers $x_1,\ldots,x_n$ and write-once output registers $y_1,\ldots,y_n$. Processes communicate through a message system which can delay a message for an arbitrary but finite time before delivery. A process fails by stopping prematurely. A run (with at most 1 faulty process) is an infinite interleaved sequence of process steps in which at most one process fails, and every non-failing process takes infinitely many steps. S solves the consensus problem if

1. (Termination) $\forall \vec{x}\ \forall \text{runs}\ \exists j$: y_j is written
2. (Agreement) $\forall \vec{x}\ \forall \text{runs}$: y_i, y_j written $\Rightarrow y_i = y_j$
3. (Non-triviality) $\forall y \in \{0,1\}\ \exists \vec{x}\ \exists \text{run}\ \exists j$: y_j written and $y_j = y$.

Theorem: The consensus problem has no solution.
Since this problem can be solved in practice, the theorem illustrates potential shortcomings of VLSI simulation models which ignore timing considerations. Study of the proof should give insight into timing properties that might be incorporated into future models to avoid such limitations.
(joint work with N.A. Lynch and M.S. Paterson)

J.-M. DELOSME:

Mapping of Algorithms onto VLSI Architectures

The task of deriving algorithms and architectures that meet the objective of performing a task in real time and with minimal latency is of practical importance. Algorithms and architectures can be developed simultaneously; the basic recursive identities exploited by an algorithm are translated into recursions on functional architectural blocks, which in turn define the data movement through an array of elementary blocks or processors and the functions of the processors. As an example we consider the case of matrix factorization.

A. MEIER:

Using a GRID FILE for Managing VLSI Design Data

We consider spatial objects as points in higher-dimensional space (e.g. rectangles in the plane: 4-dimensional record space). The search region for point location, range queries or joins is cone-shaped. The GRID FILE, a multi-key access structure, allows an efficient enumeration of all points inside, outside or on the boundary of such cones. A point location requires 2 disk accesses, a range query or a join at most 2 disk accesses per data bucket retrieved.

L. CARTER:

Practical Problems in Random Pattern Testing

The ideal VLSI testing algorithm would have small cost in terms of silicon area, performance impact and design considerations, and would allow inexpensive but accurate testing at all levels of packaging. In addition, it must be possible to field-test the replaceable units and their connectors. Current test techniques are seen to fall short of the ideal - functional testing is inaccurate, partitioning is impractical for large designs, and deterministic testing is expensive (particularly for field-testing) and doesn't model MOS faults well. Random Pattern Signature testing and design-for-testability techniques offer some hope, but there remain problems. In addition to discussing those "real world" testing problems, some annecdotal evidence is given which demonstrates that theory and practice don't always correspond exactly.

R. PINTER:

River Routing and Routability Analysis for Purposes of Placement/Compaction

River routing is the problem of laying out wires in a plane (i.e. one layer) subject to separation and width requirements. First we review the analysis of the situation for routing wires across a "smooth" channel, and show how to capture routability conditions with linear inequalities (constraints) of the form $x_i - x_j \geq a_{ij}$. Then we extend the derivation to deal with single-sided connections and "ragged" ("bumpy") sides. These features still give rise to routability constraints of the same form; however, they complicate the situation in two ways:

1. there are more constraints in the system due to the interaction between the single-sided connections;
2. choice - there are exponentially many ways to interleave the "peaks" of two opposite single-sided contours.

A problem closely related to 2. is NP-complete, but it remains open whether the additional structure present could change this status.

(joint work with C.E. Leiserson)

M. FONTET:

Recursive Layouts of Graphs

We present a way to implement the Leighton strategy for recursive layouts of graphs in the context of circuit layouts (cells and nets). By the way, we give some evidences that this strategy is far away from being usable to get acceptable layouts of circuits, even with a more accurate theorem for getting fully balanced decomposition trees from decomposition trees as we did.

(joint work with G. Varenne)

R. KOLLA:

On the Transformation of Recursively Defined Logical Networks into Electrical Networks

It is well known that for many boolean functions we can find short definitions using recursive equations. These recursive equations can be used to define planar logical networks by recursions on morphisms in x-categories. In this talk we demonstrate by an example that such recursions can be transformed into recursions on morphisms in bi-categories to obtain electrical networks. In this context electrical networks are networks which contain power supply in addition to "functional" wiring. We compare a method which transforms any x-categorial specification with the transformation of recursive specifications and point out some problems in this context.

P. MOLITOR:

Complete menus

We consider nets constructed out of a set M of cells and try to find a set R of relations with the property, that each transformation of such a net, which doesn't change the semantics, can be done according to these relations. The following demands must be made for R: 1. The semantics of the nets is invariant under the relations; 2. R is complete and finite. These demands are too general! Therefore we restrict the set M as follows: $M = M_1 \dot{\cup} M_2$, where M_1 is a set of cells, whose interpretations aren't known and M_2 is a set of cells, whose interpretations are known. Def.: R is complete, iff ($\forall$nets m_1, m_2): $m_1 = m_2 \pmod R$ $\Leftrightarrow$ m_1, m_2 are equal under all interpretations of the cells $c \in M_1$. The problem was solved by Hotz (1965) and Claus (1970) for x-categories. We generalize this result by considering nets, where the ports are in the south, north and in the west and east. The problem seems to be unsolvable, if one doesn't restrict M_1. For the special case $M_1 = \emptyset$, we get

Thm.: Let be $M_2 := \{+, \perp, \top, \vdash, \dashv, \lrcorner, \llcorner, \urcorner, \ulcorner\}$ (crossing, branches, bends) and $M_1 = \emptyset$; then there exists a finite and complete set of relations.

Berichterstatter: B. Becker

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